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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/808,258	03/24/2004	Yukihisa Takeuchi	789 123	4169

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EXAMINER	
SHERMAN, STEPHEN G	
ART UNIT	PAPER NUMBER
2629	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/04/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/808,258	TAKEUCHI ET AL.	
	Examiner	Art Unit	
	Stephen G. Sherman	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 November 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,19-33,37,39-42,46-52 and 56* is/are pending in the application.

4a) Of the above claim(s) *3-9,12,13,15,21-27,30,31 and 33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,10,11,14,19,20,28,29,32,37,39-42,46-52 and 56* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 November 2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to the amendment filed the 30 November 2006. Claims 1,2,10,11,14,19,20,28,29,32,37,39-42,46-52 and 56 have been elected for prosecution and the claims withdrawn from consideration are 3-9,12,13,15,21-27,30,31,33. Claims 16-18, 34-36, 38, 43-45, and 53-55 have been cancelled.

Response to Arguments

2. Applicant's arguments with respect to claims 1,2,10,11,14,19,20,28,29,32,37,39-42,46-52 and 56 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-2, 14, 19-20, 32, 37, 39-40, 46-50 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (US 2001/0050537) in view of Ito et al. (JP 05-325777 A).

Regarding claim 1, Itoh et al. disclose a display apparatus having a plurality of electron emitters arrayed in association with a plurality of pixels (Figure 3 shows a display apparatus containing emitters as explained in paragraph [0052].), for emitting electrons from the electron emitters to display an image, wherein:

necessary charges are accumulated in all the electron emitters in a first period (Figure 5 shows a first period Tr, where paragraph [0060] explains that the potential at the anode is floated and a scanning signal is sent on the cathodes and a display signal is sent at the same time, thus accumulating charges for display.); and

a voltage required to emit electrons is applied to all the electron emitters to cause a plurality of electron emitters which correspond to pixels to emit light therefrom, for emitting light from said pixels, in a second period after said first period (Figure 5 shows a second period Th, where paragraph [0066] explains that a voltage applied to each of

the gate electrodes during this period is a maximum level in order to permit the picture cells emitting light for display to be increased in brightness.).

Itoh et al. fails to teach that each electron emitter includes a first electrode and a second electrode in direct contact with said electrode emitter.

Ito et al. disclose of a display apparatus wherein each electron emitter includes a first electrode and a second electrode in direct contact with said electrode emitter (Drawing 2 shows that first and second electrodes 23 and 21 are in direct contact with electron emitter 22, as explained in paragraph [0017]).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to make the electron emitter taught by Itoh et al. have the configuration of the electron emitter taught by Ito et al. such that the electrodes would be in direct contact with the electron emitter in order to provide stable electron emission.

Regarding claim 2, Itoh et al. and Ito et al. disclose a display apparatus according to claim 1.

Itoh et al. also disclose the display apparatus characterized by:

a drive circuit for scanning all the electron emitters to apply necessary voltages to the electron emitters (Figure 3 shows the drive circuit 303 for scanning the emitters and circuit 302 for applying the necessary voltages.);

wherein one image is displayed in a period as one frame, said one frame including said first period and said second period (Figure 5 shows that the frame period Tf is divided into periods Tr and Th.);

wherein said drive circuit scans all said electron emitters and applies accumulation voltages depending on the luminance levels of corresponding pixels to the electron emitters which correspond to pixels to emit light therefrom in said first period (Figure 5 shows a first period Tr, where paragraph [0060] explains that the potential at the anode is floated and a scanning signal is sent on the cathodes and a display signal is sent at the same time to the gate electrodes, thus accumulating charges for display on only the cells to be lit shown in Figure 4.), and applies a constant emission voltage to all the electron emitters in the second period after said first period (Figure 5 shows a second period Th, where paragraph [0066] explains that a voltage applied to each of the gate electrodes during this period is a maximum level in order to permit the picture cells emitting light for display to be increased in brightness.);

wherein charges in amounts depending on the luminance levels of corresponding pixels are accumulated in the electron emitters which correspond to pixels to emit light therefrom in said first period (Paragraph [0060] explains the drive signal for luminescence corresponding to a display signal is sent to the gate electrodes. This means that the voltage applied will accumulate charge on the emitters and the amount will depend on the voltage sent on the gate electrode (see Figure 5).); and

wherein electrons are emitted in amounts depending on the luminance levels of corresponding pixels from the electron emitters which correspond to pixels to emit light therefrom in said second period, thereby emitting light from the pixels (Paragraph [0066] explains that a voltage is applied to the gate electrodes which allows for the continued

luminance of the display cells which are selected, meaning that the cells emit light in amounts depending on their luminance levels.).

Regarding claim 14, Itoh et al. and Ito et al. disclose a display apparatus according to claim 1.

Itoh et al. also disclose wherein said electron emitters have such characteristics that the electron emitters change to a first state in which electrons are accumulated when an electric field is applied in one direction to said electron emitters (Figure 5 shows that the voltage which is applied to the electron emitters, i.e. the selection signal is a negative voltage which would cause an electric field in a first direction.), and change from said first state to a second state in which electrons are emitted when an electric field is applied in another direction to said electron emitters (Figure 5 shows that the voltage which is applied to the electron emitters during the hold period is a positive voltage, meaning that the electric field caused by this voltage would be opposite to the electric field created during the first period.), and a drive circuit is controlled to apply a voltage between a voltage for changing the electron emitters to said first state and a voltage for changing the electron emitters to a state immediately prior to said second state, to electron emitters which are unselected (Figure 5 shows that a voltage of 0 is applied to the unselected cells, which is between –Vc and Vgmax.).

Regarding claim 19, this claim is rejected under the same rationale as claim 1.

Regarding claim 20, this claim is rejected under the same rationale as claim 2.

Regarding claim 32, this claim is rejected under the same rationale as claim 14.

Regarding claim 37, this claim is rejected under the same rationale as claim 1.

Regarding claim 39, this claim is rejected under the same rationale as claim 1.

Regarding claim 40, this claim is rejected under the same rationale as claim 2.

Regarding claim 46, this claim is rejected under the same rationale as claim 14.

Regarding claim 47, this claim is rejected under the same rationale as claim 39.

Regarding claim 48, this claim is rejected under the same rationale as claim 46.

Regarding claim 49, this claim is rejected under the same rationale as claim 19.

Regarding claim 50, this claim is rejected under the same rationale as claim 20.

Regarding claim 56, this claim is rejected under the same rationale as claim 48.

6. Claims 10, 28, 41 and 51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (US 2001/0050537) in view of Ito et al. (JP 05-325777 A) and further in view of Doyle et al. (US 5,764,205).

Regarding claim 10, Itoh et al. and Ito et al. disclose a display apparatus according to claim 2.

Itoh et al. also disclose the display device characterized in that said drive circuit comprises a pulse generating circuit for generating a pulse signal having a constant pulse amplitude (Figure 3 shows the circuit 303 and paragraph [0060] and Figure 5 explain that the pulses generated by the circuit have a constant pulse amplitude of –Vc.).

Although Itoh et al. disclose in paragraph [0060] that the voltages supplied to the gate electrodes are those indicative of the luminance level, Itoh et al. and Ito et al. fail to explicitly teach the display device characterized in that said drive circuit comprises an amplitude modulating circuit for amplitude-modulating said pulse signal to generate said accumulation voltage in said first period.

Doyle et al. disclose of electron emitters which have a controllable emission, i.e. are amplitude modulated (Column 4, lines 34-38.). The examiner interprets this to mean that in order to amplitude modulate a signal, the circuitry would need to contain an amplitude modulating circuit.

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teaching of amplitude modulation with the

display apparatus taught by the combination of Itoh et al. and Ito et al. in order to allow for the display apparatus to be able to achieve different grey levels.

Regarding claim 28, this claim is rejected under the same rationale as claim 10.

Regarding claim 41, this claim is rejected under the same rationale as claim 10.

Regarding claim 51, this claim is rejected under the same rationale as claim 28.

7. Claims 11, 29, 42 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Itoh et al. (US 2001/0050537) in view of Ito et al. (JP 05-325777 A) and further in view of Kuno et al. (EP 0 953 958 A2).

Regarding claim 11, Itoh et al. and Ito et al. disclose a display apparatus according to claim 2.

Itoh et al. and Ito et al. fail to explicitly teach the display device characterized in that said drive circuit comprises:

a pulse generating circuit for generating a pulse signal applicable to said electron emitters, said pulse signal having a voltage waveform including a positive-going edge or a negative-going edge which is continuously variable in level; and

a pulse width modulating circuit for pulse-width-modulating said pulse signal to generate said accumulation voltage in said first period.

Kuno et al. disclose of a display device characterized in that a drive circuit comprises:

a pulse generating circuit for generating a pulse signal applicable to said electron emitters, said pulse signal having a voltage waveform including a positive-going edge or a negative-going edge which is continuously variable in level (Figures 1 and 8 and paragraph [0120] explain that a pulse signal is generated from the power source +Vf/2 which contains and edge which is variable in level.); and

a pulse width modulating circuit for pulse-width-modulating said pulse signal to generate said accumulation voltage in said first period (Figure 1 and 8 and paragraph [0120] explain that the modulation circuit pulse width modulates the pulse of +Vf/2 to correspond to the gray level to be represented.).

Therefore it would have been obvious to "one of ordinary skill" in the art at the time the invention was made to use the teaching of pulse width modulation with the display apparatus taught by the combination of Itoh et al. and Ito et al. in order to allow for the display apparatus to be able to achieve different grey levels.

Regarding claim 29, this claim is rejected under the same rationale as claim 11.

Regarding claim 42, this claim is rejected under the same rationale as claim 11.

Regarding claim 52, this claim is rejected under the same rationale as claim 29.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen G. Sherman whose telephone number is (571) 272-2941. The examiner can normally be reached on M-F, 8:00 a.m. - 4:30 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SS

27 December 2006

AMR A. AWAD
SUPERVISORY PATENT EXAMINER